

## Profitable SoC Design: Using Logic NVM to Reduce SOC Costs

### *Abstract*

*Current trends in the semiconductor industry emphasize the inherent business and engineering risks associated with the development and production of a new chip. With very low incremental costs for implementing personalization design elements into system architectures, designers and technology leaders are now realizing tremendous value.*

*Methods are discussed here that illustrate the opportunities for reducing costs and maximizing economic value with new trends in system architectures. These system architecture trends are enabled by the availability of high density Logic NVM memory solutions.*

### **The High Cost of Chip Development**

Several experts in the industry place the average costs of developing an average high-end SoC at approximately \$8 and \$15 million for 130nm and 90nm designs respectively. Only an estimated five percent of design starts exceed five million units which further emphasizes the business risks associated with chip development NREs. In other words, the higher the NRE, the higher the program risk for a new design start.

As design architects look for ways to mitigate new project risk, the advantages of virtualizing a single mask set into multiple SoC products through configurable design elements becomes clear. While it is unrealistic to assume a universal chip solution for all chip designs, an intelligent approach to designing a platform architecture for a specific product category or class makes good sense. For example, an LCD TV controller chip must be designed to support a specified LCD display panel. By parameterizing its firmware and supporting multiple value-added features such as clock frequencies and display resolutions, a single LCD display controller may be made to support multiple display panels (see Figure 1). The same principal may apply to applications such as an image sensor processor or a hard disk drive controller.

In the examples described above, there are a number of cost factors to consider. In terms of development NREs, the mask costs, design, verification, and test development costs combine on a per chip basis. By approaching a product class with a single chip solution with a very low incremental unit cost adder, substantial savings may be accrued. These savings are realized in the front-end design stage as well as on the back-end in manufacturing.

In volume production, the cost benefits continue with the reduction of committed inventory stock keeping units (SKUs) down to a single device. This streamlines operations by providing the ability to personalize the device for a specific product's feature set as a last step prior to shipping to the chip vendor's customer. A single SKU may support virtualized SKU definitions without the added inventory risk and price reduction risks. These operational savings contribute directly to the company's bottom line.

On the market side of the equation, customer satisfaction is increased through faster time-to-market and faster response times to orders in manufacturing since forecasts may be aggregated across all virtualized SKUs. No longer does the product mix have to be precise.

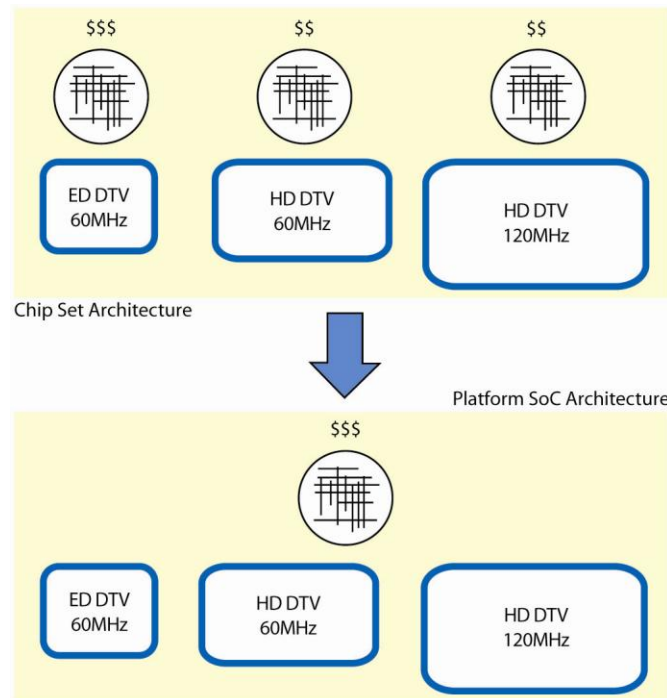


Figure 1. Platform Architecture Cost Advantage

Case 1 Example: Regarding a holistic cost comparison, there are a number of intangibles that pose challenges to illustrating a real world analysis of the benefits provided by intelligent platform architectures. Nevertheless, in review of the above, we consider an example case based on the following assumptions:

- Product SKUs = 3
- Product volume / year = 1,000,000 units (ea.)
- Product life = 2 years
- Development NRE = \$8,000,000.00 (chip1)
- Development NRE = \$3,000,000.00 (chip2)
- Development NRE = \$3,000,000.00 (chip3)
- SoC product cost = \$8.50 (ea.)
- Platform SoC product cost = \$8.65 (ea.)
- Inventory = 3 months
- Inventory turns = 4

Setting aside intangibles such as time-to-market, the development costs associated with a 3 chip program would be approximately \$14 million. By consolidating the three chips into a single platform device, a NRE cost savings of \$6 million would be realized. There is, however, a unit cost adder of \$0.15 to consider. In this case, at three million units across all three products the incremental unit cost premium would sum to \$900 thousand reducing the combined savings to approximately \$5 million. If the inventory requirements were able to be reduced by half with the platform SoC product, the carrying cost savings at 6% per year would amount to approximately \$380 thousand over two years. Additional cost savings would be added due to avoiding production forecast errors, price reduction risk and inventory obsolescence.

### Manufacturability Yields Cost Savings

While in the example case provided above, the costs savings were calculated for combining multiple designs into one platform architecture, there may be substantial benefits for a single chip architecture as well. As designers contemplate 45nm and 32nm development programs, reliability, quality, and yield become primary considerations. This is due simply to increased complexity. More logic gates, more mixed signal devices, and more complex software mean more to go wrong in design, production, and post production. Of course, what does any of this have to do with non-volatile memory? The answer lays within the system architecture.

Many signal integrity issues, as well as other mixed signal issues, are rooted in sensitivities due to variations in process or physical fiber, cables, or connectors. These physical layer related sensitivities may manifest themselves as functional, reliability, or quality issues with imaging, RF, environmental sensor, and/or signal integrity circuits. As engineers push the physical limits of advanced process geometries, the importance of on-chip one-time programmable (OTP) memory increases.

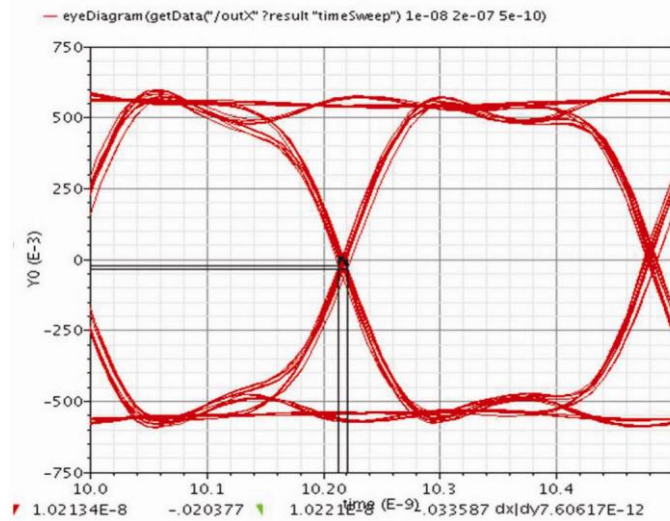


Figure 2. Programmable Signal Integrity Control

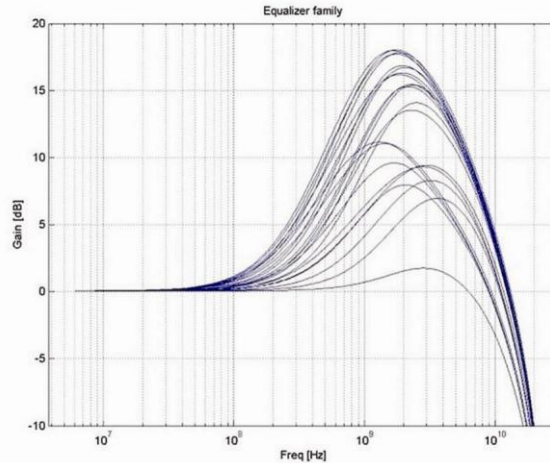


Figure 3. Programmable Adaptive Equalizer

Case 2 Example: For HDMI which requires high bandwidth digital transmission of audio and video information, signal integrity directly translates into a high quality entertainment experience (The images and example information illustrated in figures 2 and 3 are provided, with permission, by the Transwitch Corporation.) If there are signal integrity issues, the HDMI chip will not yield well for a high volume consumer application. Therefore, the ability to architect programmable HDMI signal attributes such as amplitude, slope, pre-emphasis, and termination impedance has a direct impact on manufacturability. Additionally, the same is true for designing an adaptive equalizer into HDMI which enables the HDMI chip to accommodate a wide spectrum of cables and speeds. These types of signal parameters may be programmed uniquely for each HDMI device.

In reference to the assumptions in the Case 1 Example above, if a single percentage point in die yield is saved, the resulting cost savings would amount to \$510,000. This does not take into account intangibles such as increased customer satisfaction.

While this example has focused on HDMI, there are many applications which benefit in the same way. Many SoC applications benefit from the ability to store state change information on-chip for calibration, adaptive tuning and self-repair types of applications.

### On-Chip vs. Off-Chip Cost Savings

Traditionally, non-volatile memory technologies have required a non-CMOS process. That is, the memory bit cell requires a new or modified process inherently different than a logic transistor. EPROM, EEPROM, and Flash are good examples of memory process technologies that are fundamentally different than standard logic CMOS. With new innovations and inventions there are now three non-volatile memory technologies in standard logic CMOS:

- Electric Fuse
- Antifuse
- Floating Gate

For the scope of this discussion, a detailed description of each type of technology will not be provided. More recently the CMOS antifuse has enabled high density embedded non-volatile memory in standard logic CMOS. Due to the relative decreased size of the bit cell compared with the other two technologies, SoC applications now have access to low cost, high density NVM on-chip. The primary alternative for storing digital information on-chip is, in fact, an EPROM, EEPROM, or Flash discrete memory device. There are two case models for a comparative cost analysis: 1) an NVM device is part of the system design and available with no incremental system cost, and 2) an NVM device is needed only to support the SoC and is not provided as part of the system requirements.

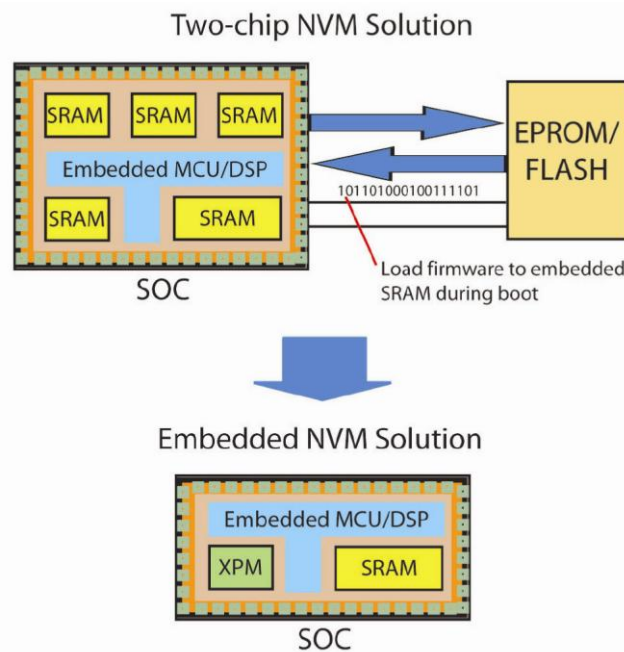


Figure 4. Two-Chip vs. One-Chip Configuration

In some SoC applications, even with the availability of system NVM such as Flash, information must be stored on-chip due to the sensitive nature of that information. Chip ID, manufacturing codes, encryption keys, boot code and proprietary firmware parameters are good examples. In other cases, the SoC may have multiple use cases that include systems with and without NVM such that the SoC must embed the NVM or include in a stacked packaging configuration.

For the case in which system NVM is considered “free”, the Flash device is already built-in. In this case, the argument for embedding NVM would come in the form of intangibles which are more difficult to estimate. For example, design IP protection or third party data content protection may require a cost premium. The benefit may or may not be realized unless there is an unwarranted attack that results in damages to the chip vendor or their customer. For the case of off-chip NVM, there will still need to be SRAM for storing the information loaded from the off-chip NVM device. In this case, the embedded NVM competes directly with on-chip SRAM in terms of die area and performance.

Comparing the cost of and embedded NVM IP module to a stacked chip configuration is the most likely cost comparison. In this case, the cost of the IP, the IP integration, the die area consumed by the IP module, and cost of programming are compared with the cost of the discrete NVM die, memory testing, incremental packaging, incremental assembly yield loss, and programming. The example described in Table 1 below assumes a design requirement for a 128Kb embedded NVM IP module on a 65nm process node. All other project assumptions are the same as for the Case 1 Example above.

	Embedded	Stacked (Discrete)
IP cost per chip	\$0.04	-
Die/test cost	\$0.06	\$0.13
Packaging (incr.)	-	\$0.28
Pkg yield loss (incr.)	-	\$0.02
Programming cost	\$0.03	\$0.01
Total per chip	\$0.13	\$0.44
Total production	\$780,000.00	\$2,640,000.00
Emb. NVM Savings	\$1,860,000.00	-

Table 1. Embedded vs. Stacked Package Cost Comparison

As indicated above in Table 1, the costs are compared between a stacked (two chip) approach and an embedded (one chip) approach. The resulting cost savings with the single chip approach total to over \$1.8 million.

**What to Consider for an Embedded NVM Solution — Manufacturability, Ease of Use, & TCO**

As with any IP solution, the designer must make sure that the foundry supports the underlying IP. This is particularly true of logic NVM IP since all existing logic NVM technologies utilize standard logic CMOS structures in ways unintended by the wafer manufacture. This fact emphasizes the importance of qualification support by both the logic NVM IP vendor and their wafer foundry partner.

Additionally, it is important to understand the ease of implementation and manufacturing. There should be negligible yield impact which evidence is clear when the underlying technology is mass produced. Newer technologies should be well understood from both a yield and reliability perspective.

Another consideration is flexibility. Does the technology and IP vendor support multiple process nodes? Is the IP product field programmable? Is the required configuration available off the shelf or is there a lead time to consider? Are there hidden costs due to tradeoffs of the underlying logic NVM technology? The IP vendor should be able to provide details including qualification data, foundry contact support, and additional customer references if asked.