Kilopass Embedded XPM Technology:
A New Field Programmable Non-volatile Memory

A Technology Backgrounder

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Non-volatile Memory Technologies

Embedded non-volatile memory has always been a critical requirement for SoC designers. Applications requiring code storage, encryption keys, serialization, trimming and permanent data storage all use some form of non-volatile memory. There are five competing technologies available for implementing non-volatile memory.

1. Masked-ROM
2. Fuse
3. Floating gate devices such as EPROM, EEPROM, or FLASH
4. Embedded FLASH
5. Gate Oxide Anti-fuse

Each of these technologies has its own advantages and drawbacks.

	ROM	eFlash	Fuse	Floating Gate	Kilopass (AntiFuse)
Process R&D Cost	$1M	$25M	$5M+	$5M+	**$1M**
128kb in 65nm (normalized)	0.2	1.5	32	Not scalable	**1**
Field Update	No	Yes	No	Yes	**Yes**
Security	Low	Low	Low	Low	**High**
Extra Board Space	No	No	No	Yes	**No**
Reliability	Excellent	Poor	Medium	Poor	**Excellent**
Design Cost/Risk	Low	High	Low	Medium	**Medium**

1. Masked ROM (Read Only Memory)

ROM data are printed into the SoC during fabrication of the SoC. ROM is smaller in size comparing to other technologies. It has good data retention time. The drawback of ROM is the long fabrication turnaround time. If the ROM data needs to be updated, it usually takes months and requires mask changes.

2. Fuse

Foundry fuse technology is a one-time programmable memory that mainly uses silicide on poly line to alter the resistance.

The most commonly used fuse is Poly/Metal Fuse. Poly/Metal Fuse can be programmed by applying a high voltage source across the fuse. Laser Fuse makes use of a Laser beam for programming.

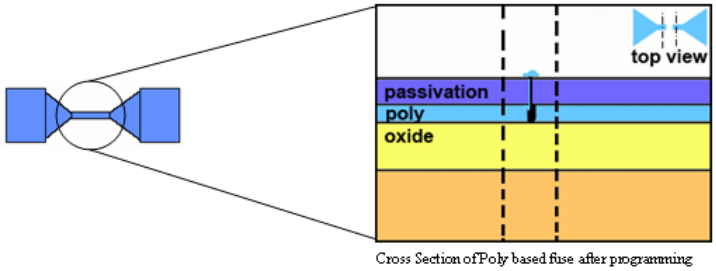


Figure 1: Poly/Metal Fuse

Most fuses can only be programmed at wafer and have stringent power requirements for programming. It makes programming in packaged parts difficult. Another drawback of the fuse is that the size of fuse increases linearly with the number of bits implemented. For higher bit density memory applications, e.g. greater than 2K bits, the size of the fuse quickly begins to take up the area of the Soc. Fuse is usually provided by the foundry and cannot be legally ported to another foundry without the consent of the foundry.

3. Floating Gate Devices

External floating gate devices like EPROM, EEPROM or Flash are another type of NVM. One way to implement floating gate devices is to design a CMOS transistor with two overlapping gates. Charges are stored in the floating gate by applying a high voltage source via a mechanism known as Fowler-Nordheim tunneling effect. The presence or absence of charges in the floating gate determines if the transistor is on or off during read operations. Thus, a “1” or “0” is detected accordingly. The advantages of floating gate devices is it can be erased and electrically programmed multiple times, up to 100K times.

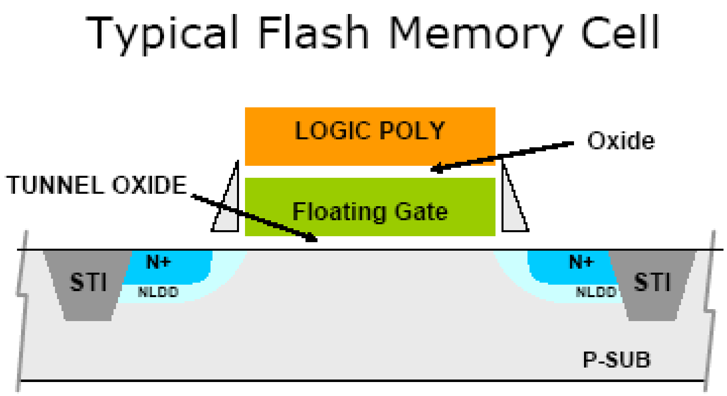


Figure 2: Floating Gate Device

The overlapping gate oxide layers require additional masks and processing steps to standard CMOS logic process. That is an added cost to manufacturing. Another drawback is the lack of migration path to process technologies smaller than 0.13um. The more advance technologies have high leakage and makes the stored charges in the floating gate more difficult to retain. The data retention issue is more severe when the temperature is high.

4. **Embedded Flash**

Embedded flash is similar to external flash above except the flash is embedded in the SOC. There is a similar kind of embedded flash called SONOS. It stands for Silicon Oxide Nitride Oxide Silicon. It differs from the mainstream Flash by the use of Silicon Nitride instead of Polysilicon for the charge storage material. Again, it has the same drawbacks as Floating Gate Devices above.

5. **Gate Oxide Breakdown**

Gate Oxide Breakdown is used as one time programmable non-volatile memory. Gate Oxide Breakdown is achieved by applying a high voltage to the gate of a transistor while keeping a low voltage at the source side of the transistor.

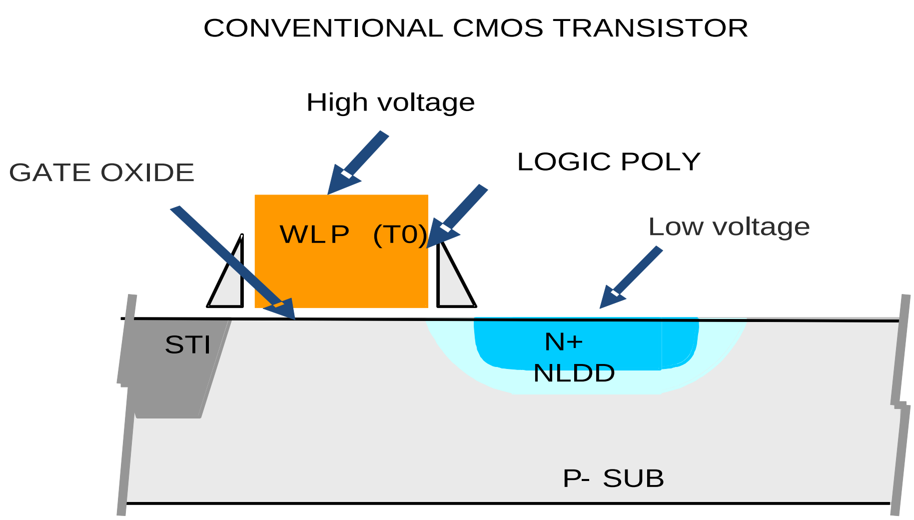


Figure 3: Gate Oxide Breakdown

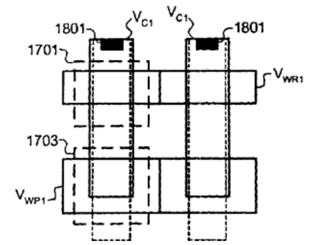
Before the breakdown, between the gate and the source of the transistor, it is isolated like a capacitor. After the breakdown, it behaves like a resistor between the gate and the source. The advantage of the Gate Oxide Breakdown technology is that the bit cell size is small, with only 2 transistors per bit cell. The programming can be done in wafer or packaged parts. Sensitive data stored using this technology is physically secure and has proven to be economically infeasible to break into. Gate Oxide Breakdown is applied with standard CMOS. There is no additional cost associated with additional masks or processing steps. It has been proven in 0.18um, 0.13um, 90nm, 65nm and 40nm. Density and performance characteristics improve with smaller process geometries. Gate Oxide Breakdown technology has a wide operating temperature range and is radiation hardened. The drawback of this technology is that it can only be programmed once.

Kilopass XPM Technology

Kilopass has 19 patents covering 230 claims. The patents can be broken up into 3 different technologies:

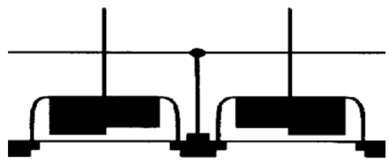
1.5T/2T Patents

- **US 6,667,902; 6,671,040; 6,700,151; 6,798,693; 6,822,888, etc.**



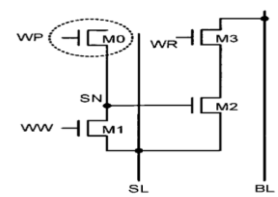
1T Patents

- **US 6,992,925, US 6,940,751, US 6,856,540, US 6,898,116, US 6,777,757**



3.5T Patents

- **US 7,173,851**



Kilopass's XPM product is based on the 1.5T/2T bitcell patent for manufacturability and reliability. Kilopass eXtra Permanent Memory (XPM) non-volatile memories are based on Gate Oxide Breakdown technology. The XPM bit cell is composed of two standard CMOS transistors. One of them is the Select Transistor (WLR) and is the other is the Program Transistor (WLP).

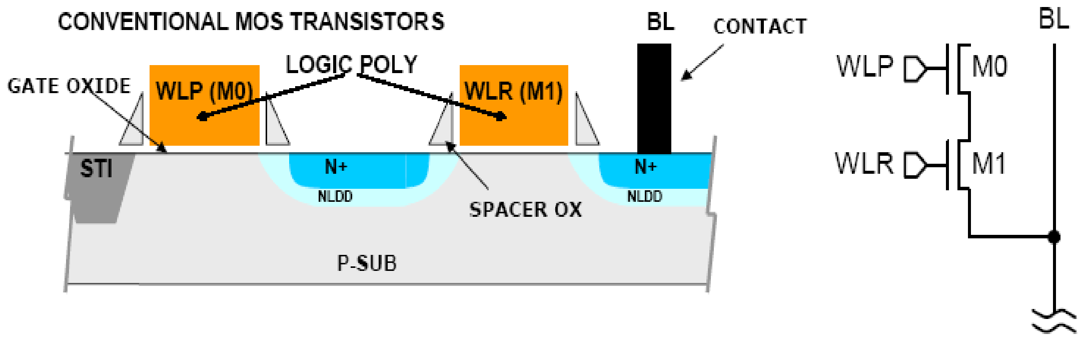


Figure 4: Bit cell before Programming

Before programming, the gate and the source side of WLP are isolated. No current flows through **WLP**. During programming, a high voltage is applied to the gate side of WLP with WLR selected. The bit line (BL) is kept close to ground. The high voltage across WLP breaks the gate oxide of WLP. After programming, the gate and source side of WLP behaves like a resistor.

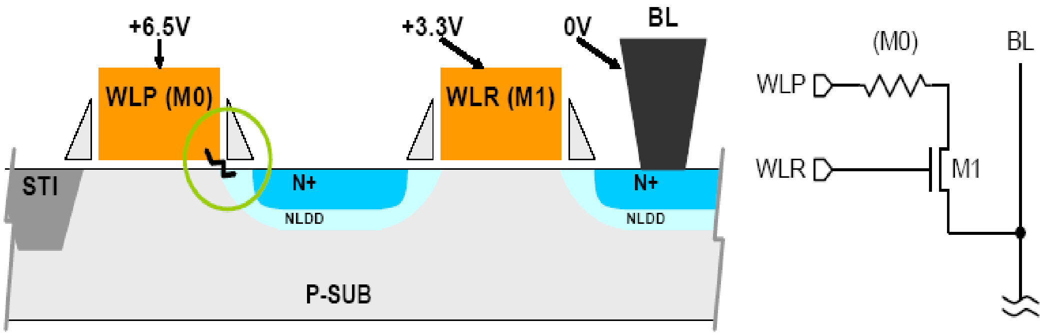


Figure 5: Bit cell after Programming

Data in the bit cell before programming is a "0". After programming, the data is now a "1". The fact that Kilopass bit cell is "1" or connected after programming classifies Kilopass bit cell as "anti-fuse". The Kilopass innovation is a very short channel MOS transistor with its gate connected to its drain. It has a finite turn-on voltage, in the low hundreds of mV, and finite impedance, on the order of tens of Kohms. The memory can be programmed with an externally provided programming voltage supply or an on-chip charge pump. Important to power sensitive applications, the XPM cell has a low programming current.

Low cost of ownership

Kilopass XPM bit cell is composed of two short channel standard CMOS core transistors. The size of the bit cell is very small comparing to other technologies. This leads to smaller overall size of the memory module. XPM modules are designed using only standard CMOC logic process. There is no additional MASK layer or process step required. Both factors make up a very low cost of ownership.

XPM Reliability

From a reliability standpoint, the anti-fuse must be able to withstand an un-programmed bit, a zero, from getting programmed, and a programmed bit, a "1", from flipping back to a "0"; undoing the anti-fuse connection. Temperature, voltage, or read operations do not degrade the XPM cell's reliability as they do with other NVM technologies. Kilopass XPM technology's immunity from these failures has been demonstrated in standard reliability testing using high temperature and high voltage acceleration like High Temperature Operation Life (HTOL) tests. The devices were subjected to elevated temperatures of 125°C and a heightened voltage of 40% over nominal. In this accelerated life test environment, the memory was subjected to cycling read operations up to 1000 hours. Additionally, Kilopass performed a Data Retention Bake (DRB) test commonly used in testing non-volatile memories. The memory device is placed in an oven at 150°C for 1000 hours to see if any of the cells bake out and fail. In both cases, the test determines whether or not the XPM cell degenerates and creates an open circuit or exhibits a significant shift from its nominal characteristics. The Kilopass XPM technology passed both tests with no signs of failure or degradation. Kilopass XPM memories are qualified in major foundries including TSMC, Chartered, SMIC and Dongbu. Qualification reports are available for all qualified process nodes. Please contact your sales support or application engineer for copies.

In addition, Kilopass XPM technology has been used in many of the customers' products in production. The technology has been field proven to be reliable for mass production.

XPM Security

Storing secured information, like encryption keys, has always been a challenge in the information world. Attacks on sensitive information stored in SoC can come in many different forms; probing, microscopy, voltage contrast, fault induction, reverse engineering and others. Kilopass XPM has been proven to be safe from these physical attacks.

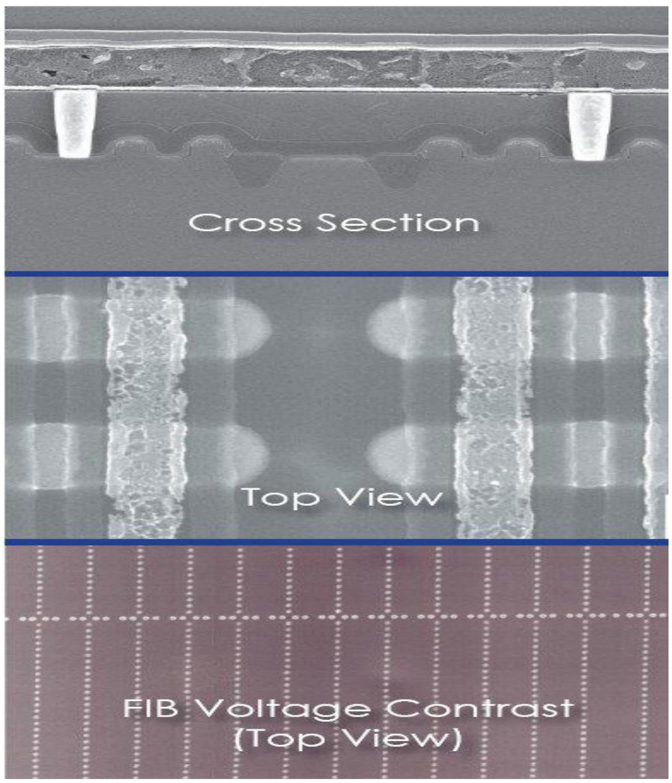


Figure 6: XPM with checker board pattern

Figure 6 shows the checker board pattern used to program the devices used in all three photographs. This is due to the inherently small size of physical changes that occur to the CMOS transistor's gate oxide when programmed from its original "0" state to a programmed "1" state. Since the oxide break-down occurs in a random location within a bounded enclosure, and is extremely small, the state of the bit cell stays well hidden in the CMOS silicon atoms. Likewise, because there is no charge stored as with Flash, EPROM, or E2PROM technologies, there is no charge to detect as a "1" or "0" state.

Kilopass Register and Memory Products

The Kilopass XPM product family is available in 16bit registers and memory blocks from 1Kbit to 1Mbit. The 16bit register offers a 'fuse' architecture with 16 bits in a block. It may also be cascaded multiple times to form a multiple of 16 bits of storage. See Fig. 7 below for a diagram of three 16 bit XPM registers cascaded together.

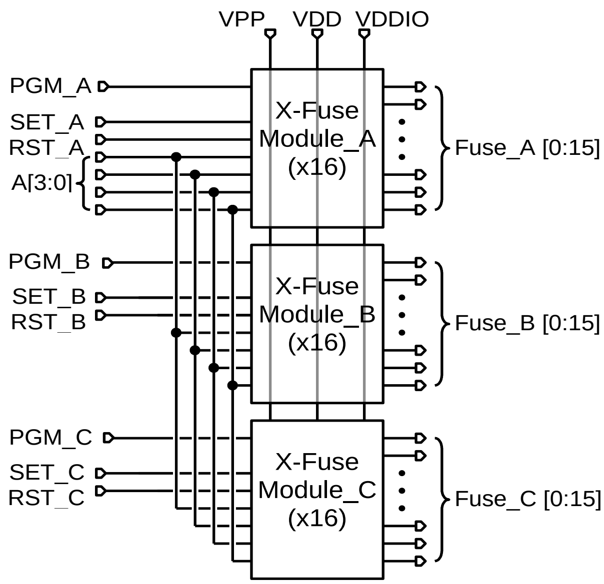


Figure 7: Cascaded 16bit registers

Kilopass memory products are available from 1Kbit, 8Kbit, 64Kbit… up to 1Mbit densities. Below is a Kilopass memory block diagram.

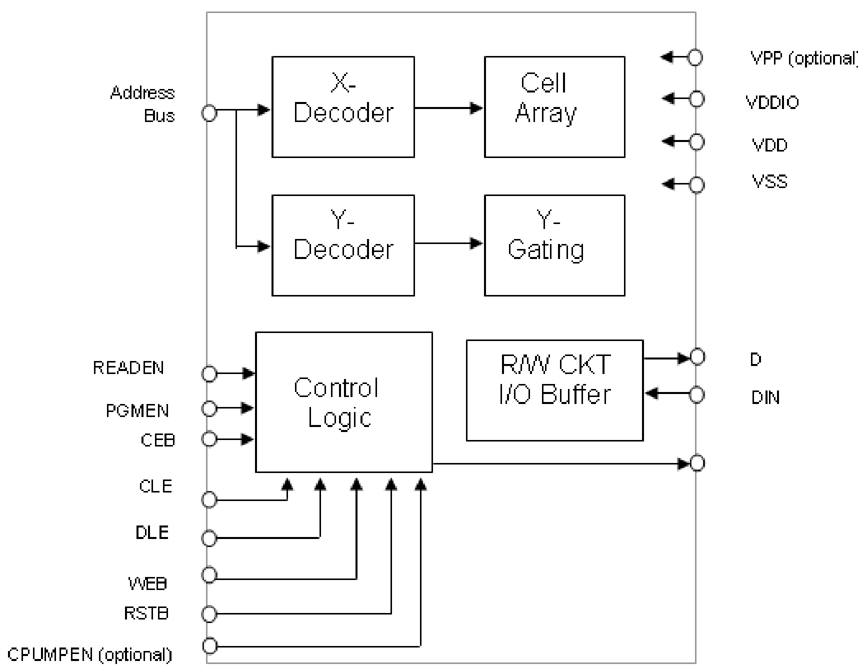


Figure 8: Kilopass Memory Block Diagram

All Kilopass products come with built-in tests that are Design for Manufacturing (DFM). There are 4 DFM tests:

1. Blank Check
   Blank Check is the first incoming test. It reads out all the bits at a specified voltage to

make sure there is no defective bit in the product. This verifies the memory array is good to program under the product operating conditions.

2. TestDEC
   TestDEC tests the support logic including address decoders, bit lines, sense amps and others. This verifies no stuck at zero or one bit lines or address lines.
3. Write Test
   Spare rows of XPM bit cells are embedded into the module. The spare rows can be used for pre-programming to verify that the programming mechanism (such as the charge pump or VPP pads) is working. Programmed bits will be read and compared to verify that the programmed data are correct. This is done before the main memory cells are programmed.
4. Program Verify
   After the main memory cells are programmed, Program Verify will read back the programmed data at a specific voltage. The specific voltage emulates the worst case operating condition of the product. This is to make sure the product will work within the specification under worst case conditions.

The tests can be performed in wafer, on testers, or in customer packaged parts. This makes Kilopass XPM easy to manufacture.

Programming Voltage

The programming voltage for an embedded Kilopass memory block may be delivered via an on-chip charge pump or from an external VPP pin. The programming voltages for different processes are different. It varies from 8.5V for 0.18um process to 5V for 40nm parts. Once programmed, the memory will retain virtually forever. For customers selecting VPP pad option, a VPP reference pad with ESD structure is available from Kilopass. Kilopass tested the VPP pad for ESD and latch up. It passed HBM 2000V and MM 200V. Customers may select to design and layout their VPP pad using Kilopass VPP pad as a reference.

Kilopass

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